

# Foxconn Precision Co. Inc.

## G41M05 Schematic

Fab.A  
Data: 2008/7/30

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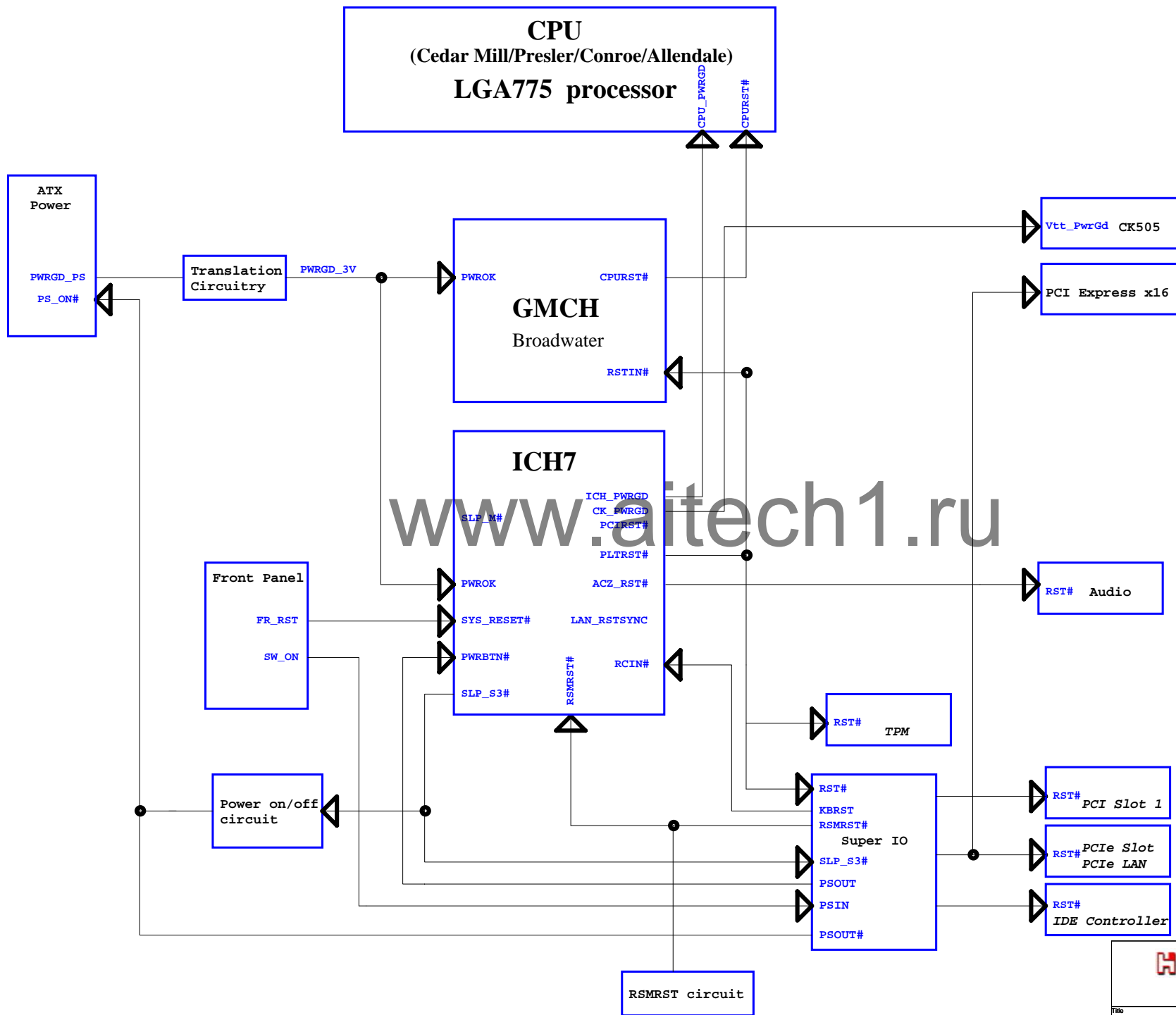
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14.318MHz

CPU

CPU 200/266/333 MHz Diff Pair

MCH 200/266/333 MHz Diff Pair

PCI Express 100 MHz Diff Pair

PCI Express x16 Gfx

DOT 96 MHz Diff Pair

G41

Channel A DDR2  
DIMM1

Channel B DDR2  
DIMM1

PCI Express/DMI 100 MHz Diff Pair

PCI Express/DMI 100 MHz Diff Pair

USB/SIO 48 MHz

ICH 33 MHz

REF 14 MHz

PCI 33 MHz

PCI Slot 1

TPM 33 MHz

TPM

SIO 33 MHz

SATA 100 MHz Diff Pair

PCI Express 100 Mhz Diff Pair

ICH7

SPI Clock

SPI

Azalia Bit Clock

HD Audio

32.768KHz

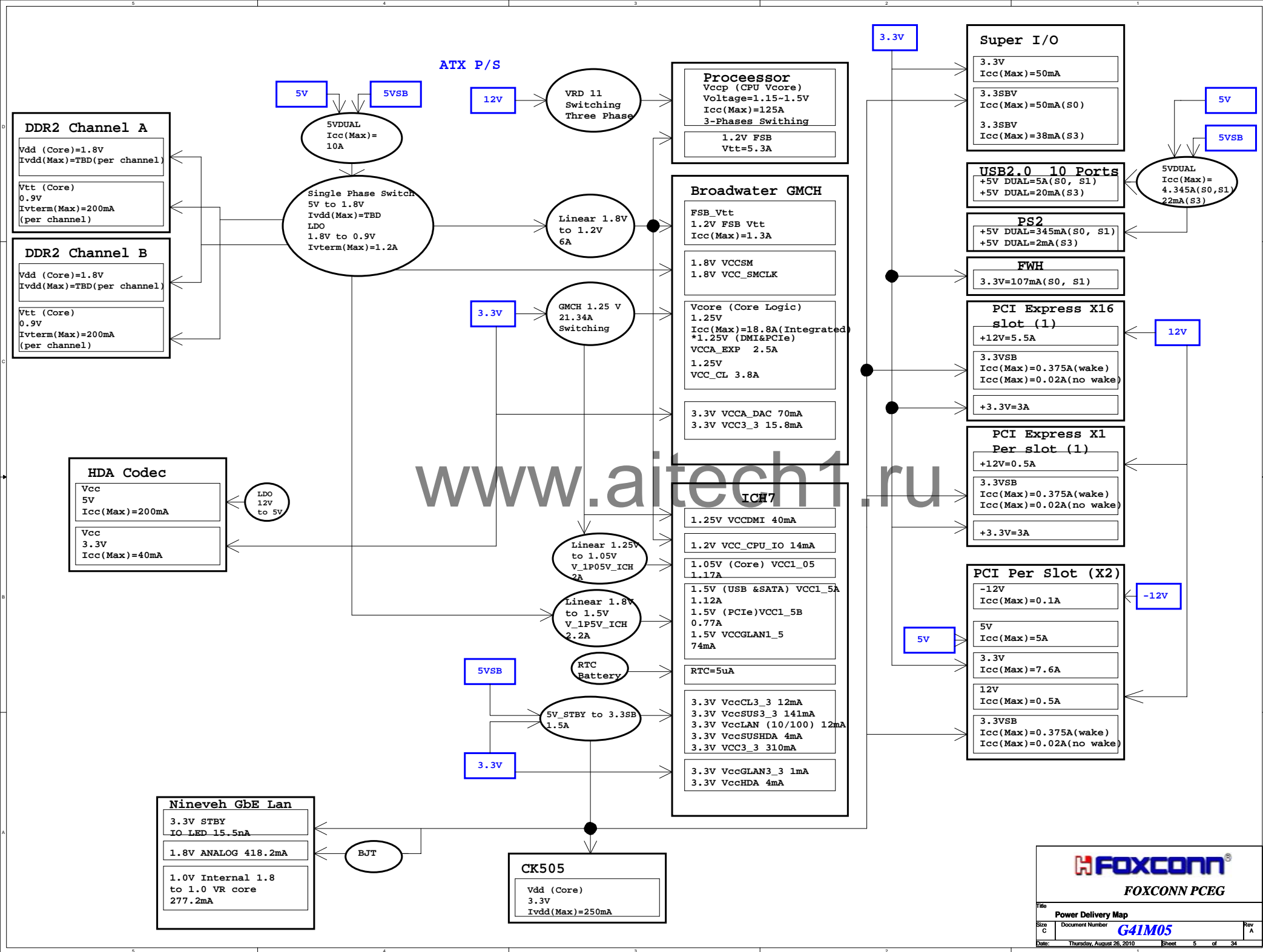
Super I/O

ICS9LPRS908DGLF

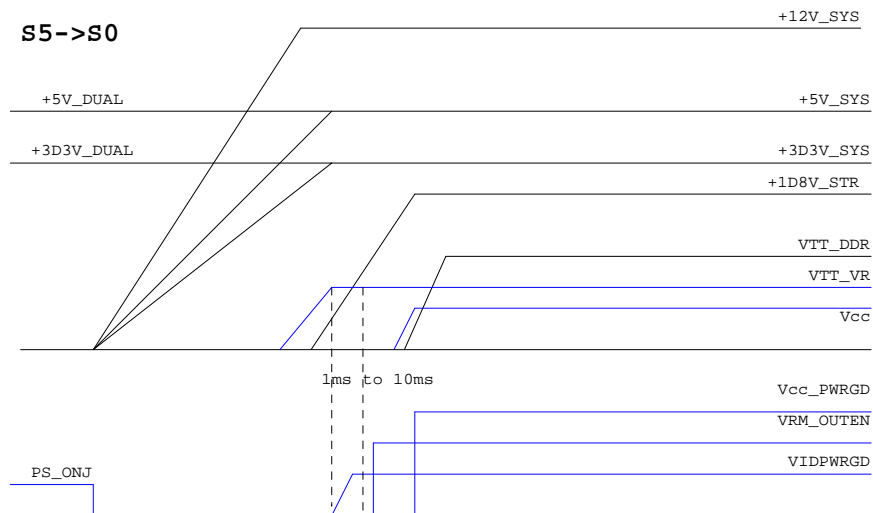
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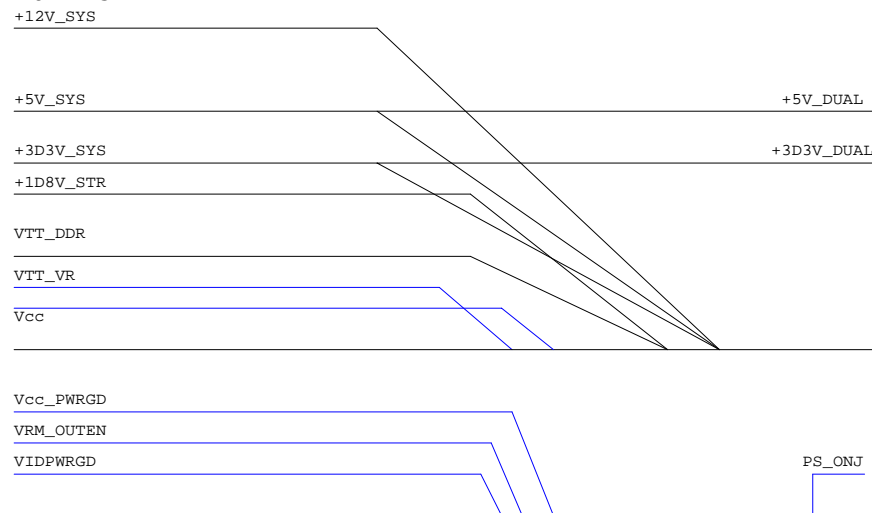
Title		
Clock Distribution		
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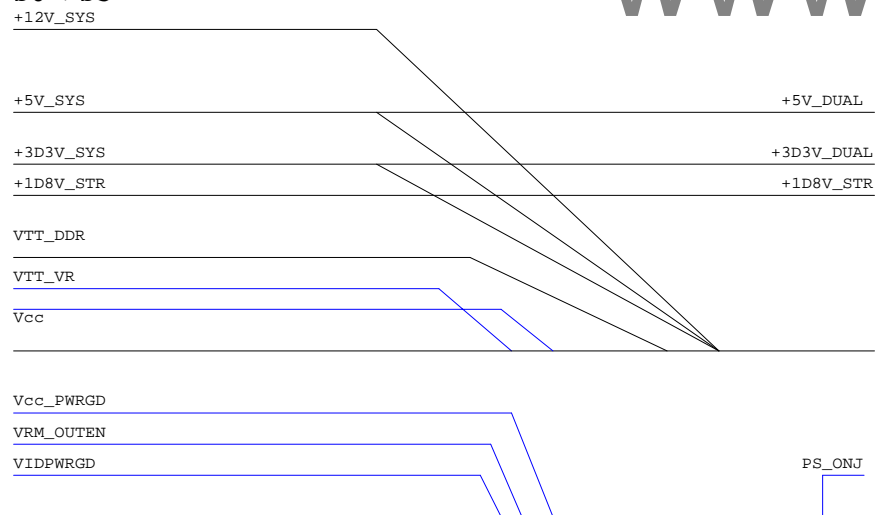
# S5->S0



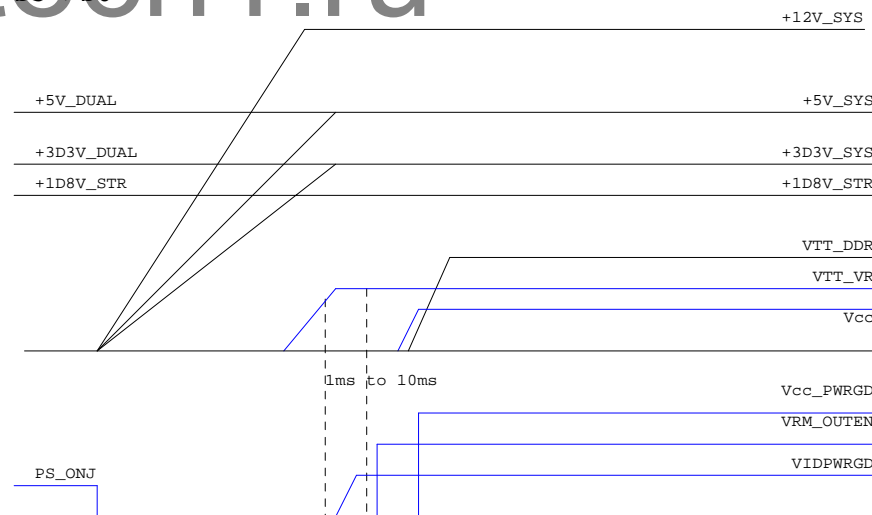
# S0->S5



# S0->S3



# S3->S0

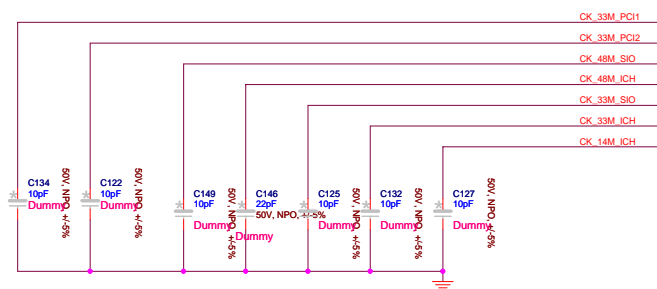
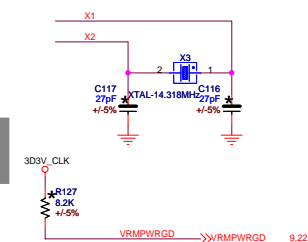
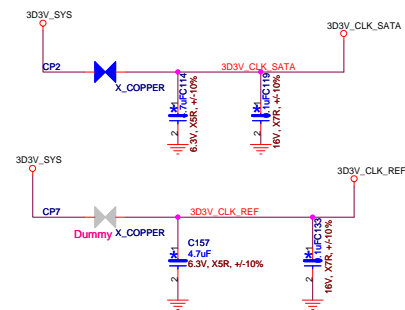


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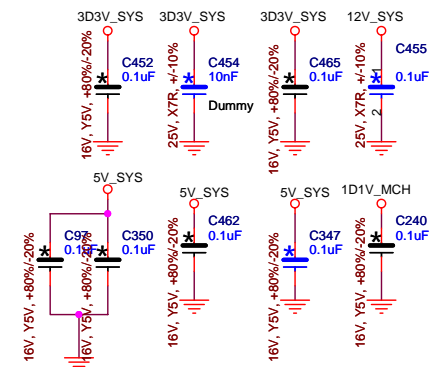
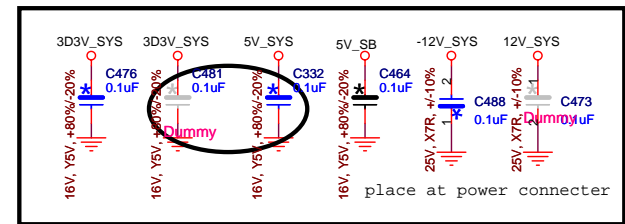


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Title <b>Power Sequence</b>		
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1	1	0	400MHz(1600)
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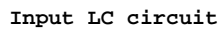


HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Power
NC	9	10	Key

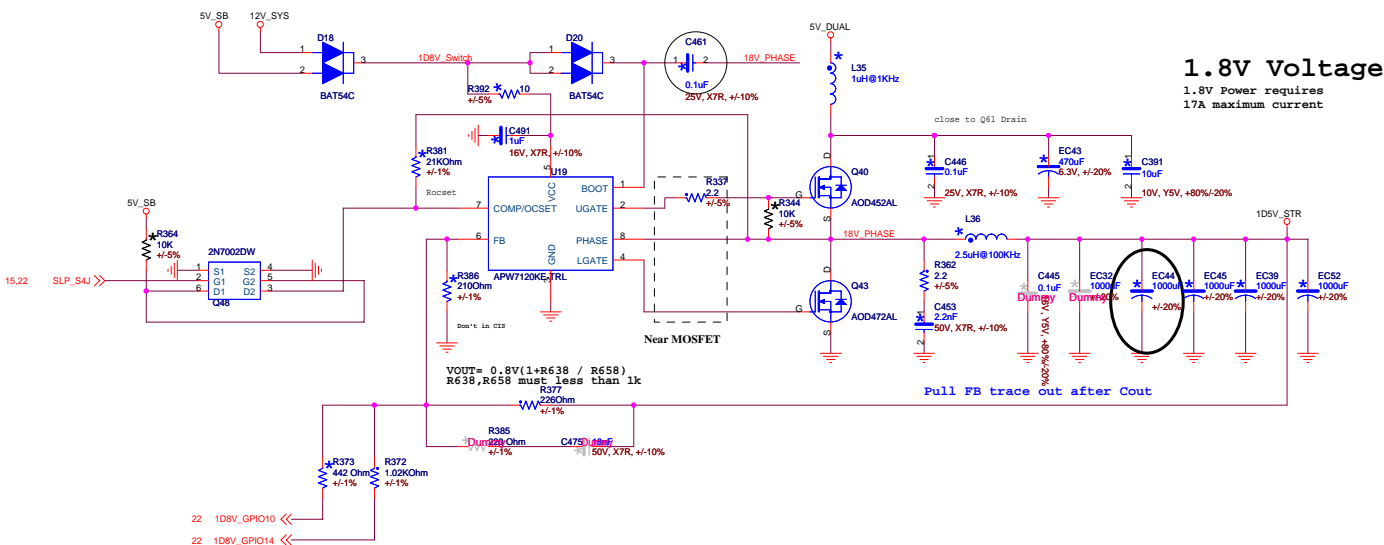


Title			
Power/MISC Connectors			
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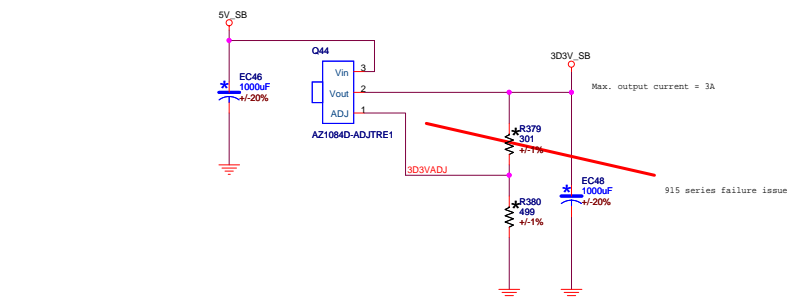
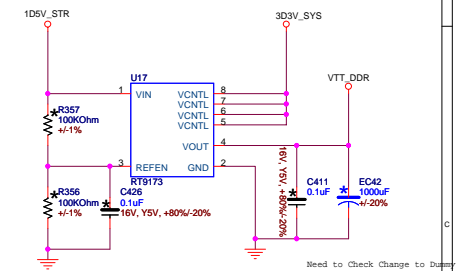






1D8V\_STR

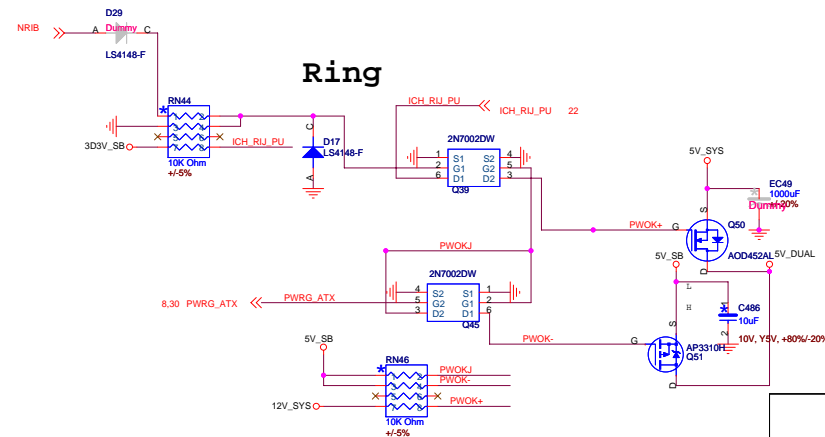
DDR\_VTT



$$V_{out} = V_{ref}(1 + R2/R1) + I_{adj}R2$$

R1 is Up Resistor.  
Iadj=50uA  
Vref=1.25V

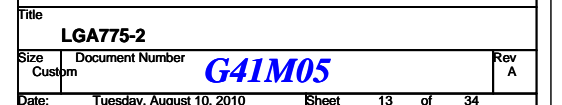
3D3V\_DUAL



5V\_DUAL

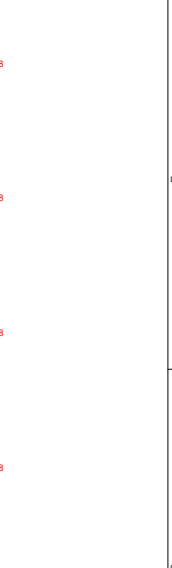
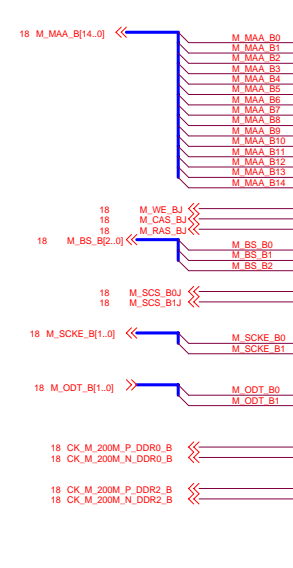


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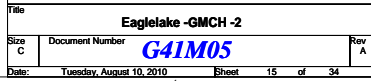
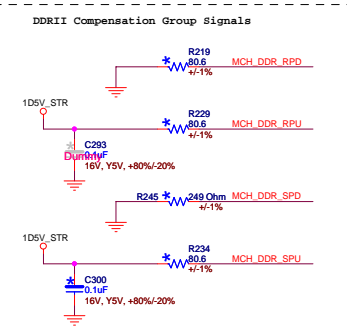


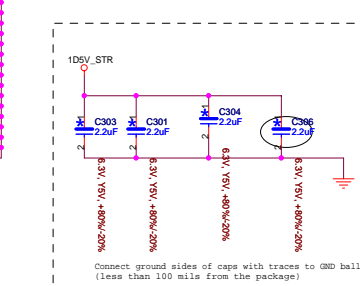
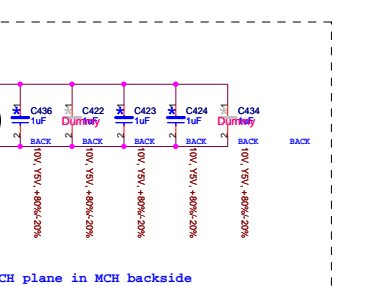
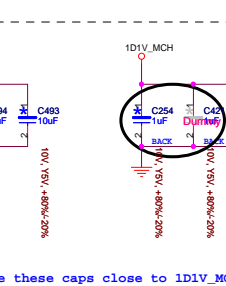
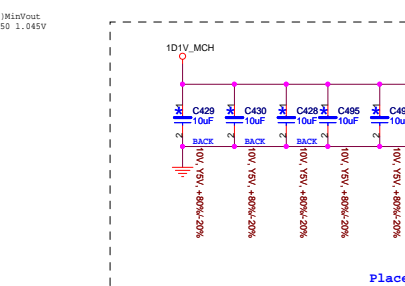




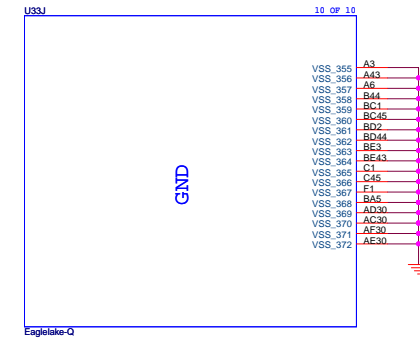
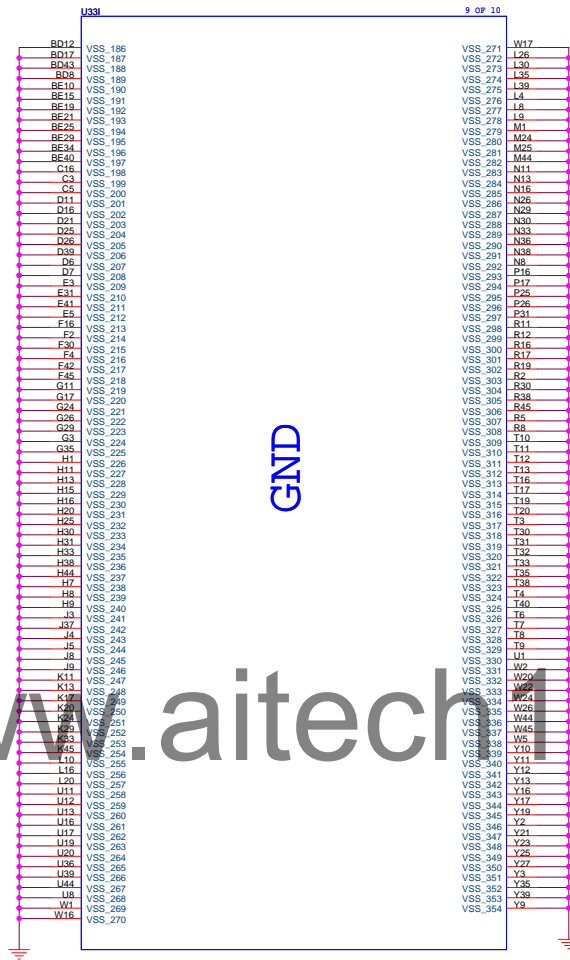
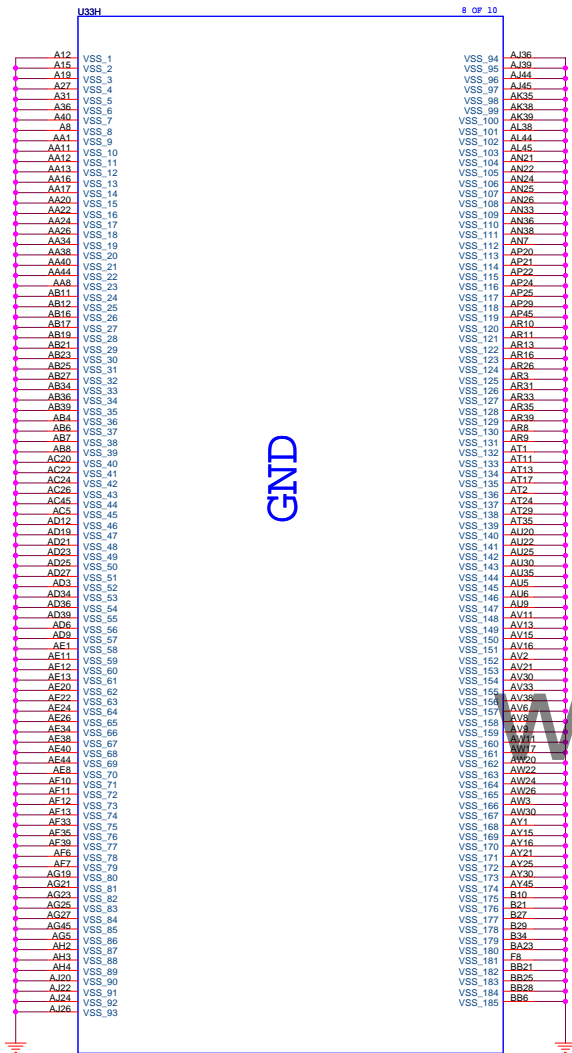


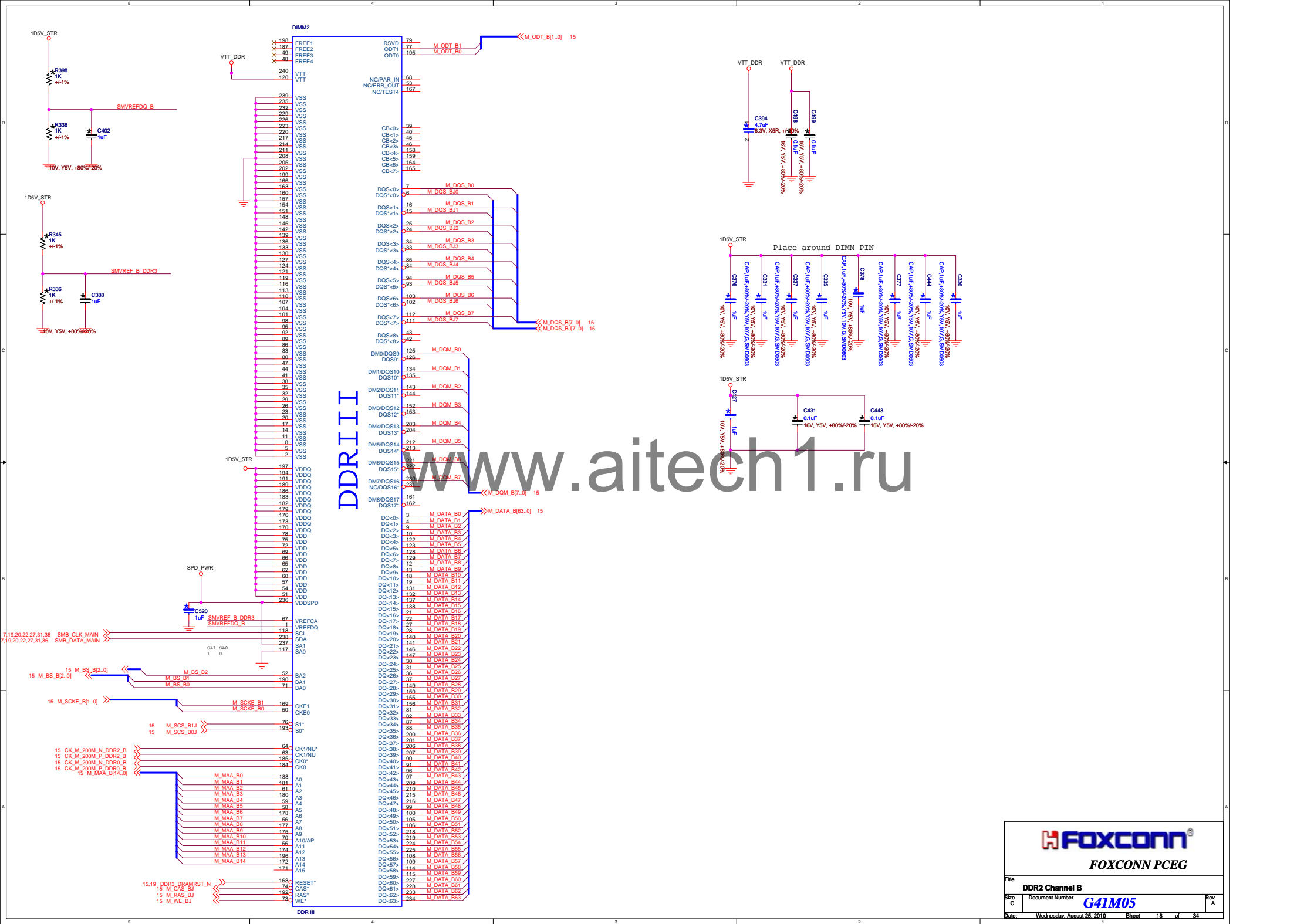
Eaglelake-Q

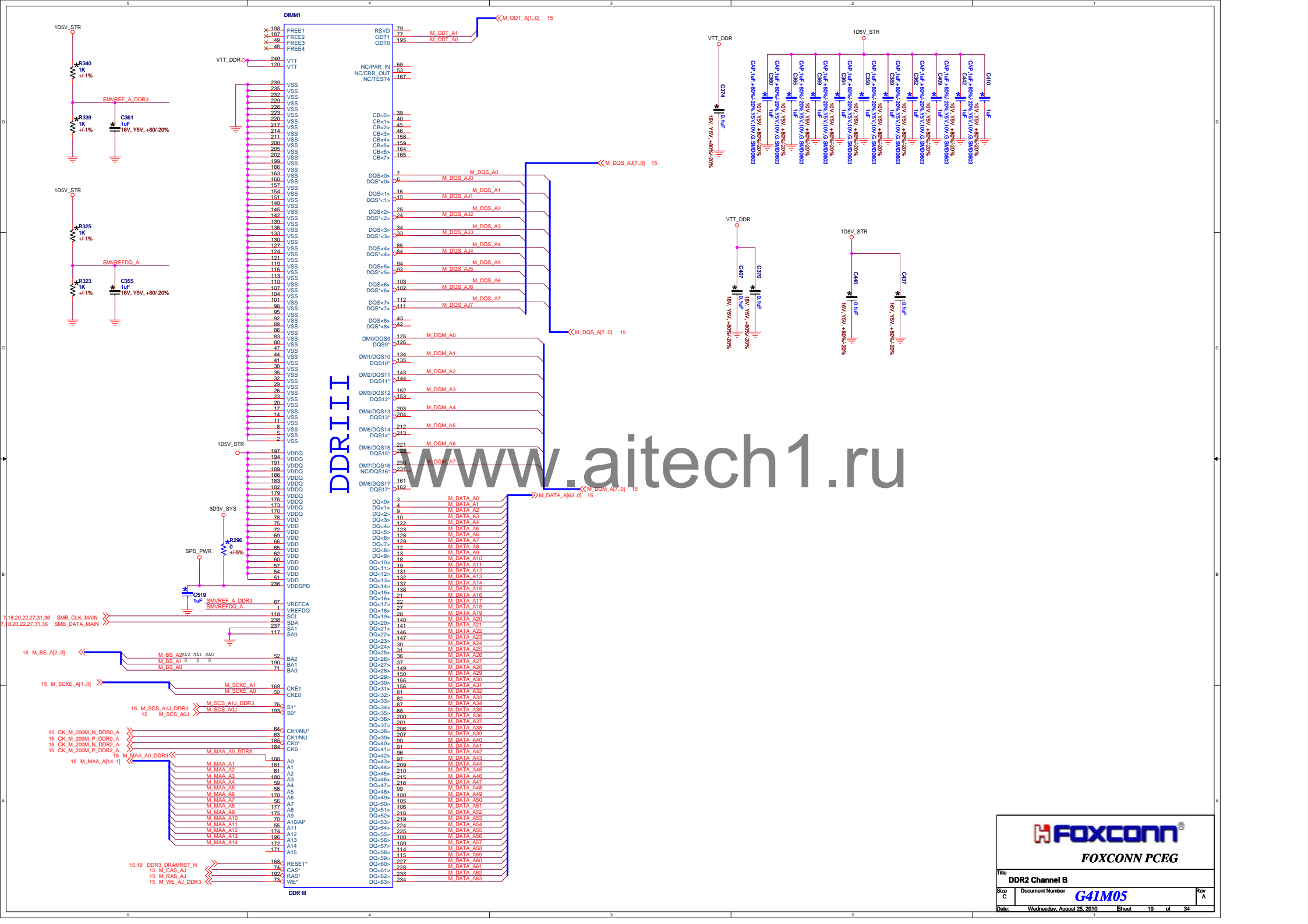


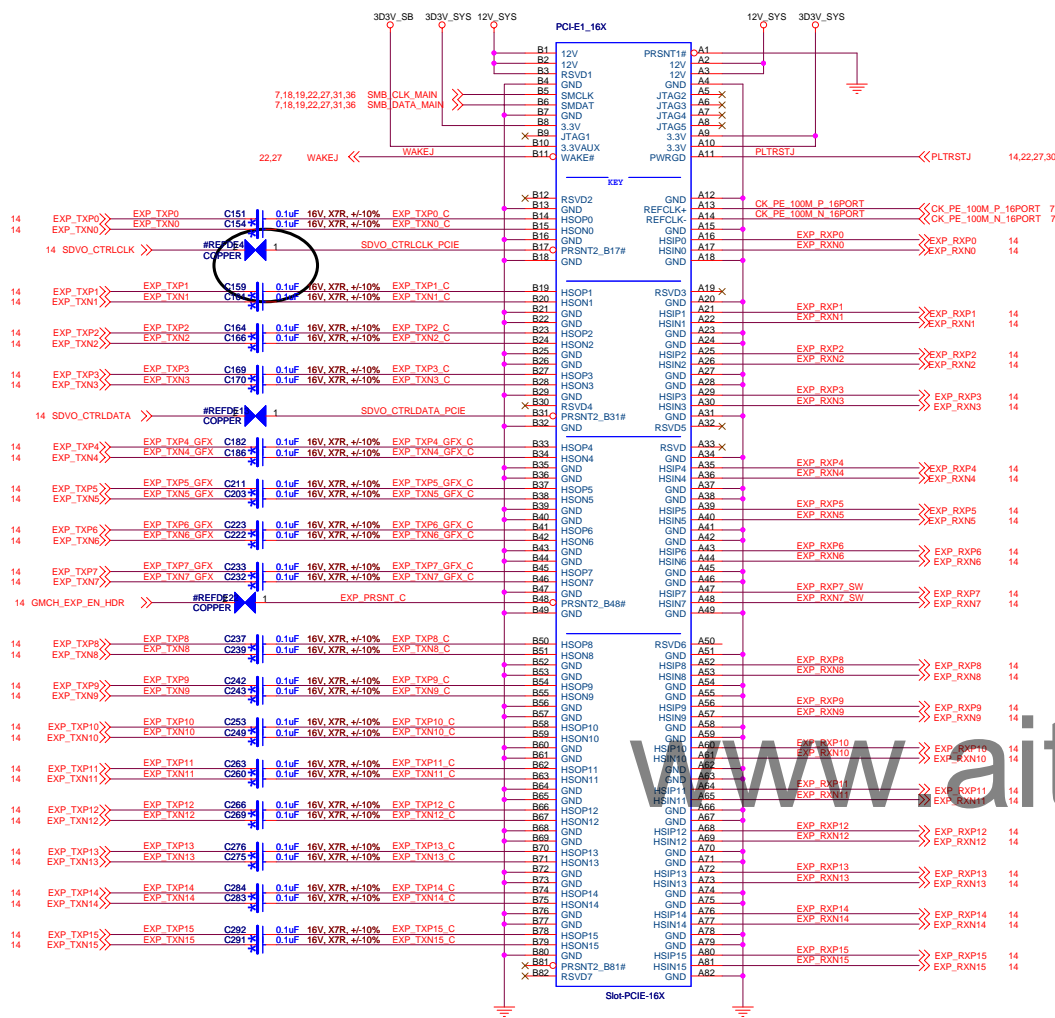




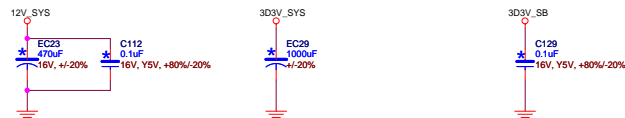


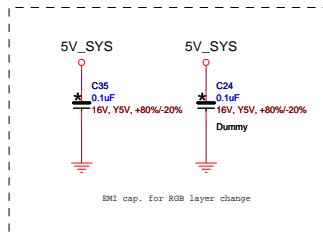






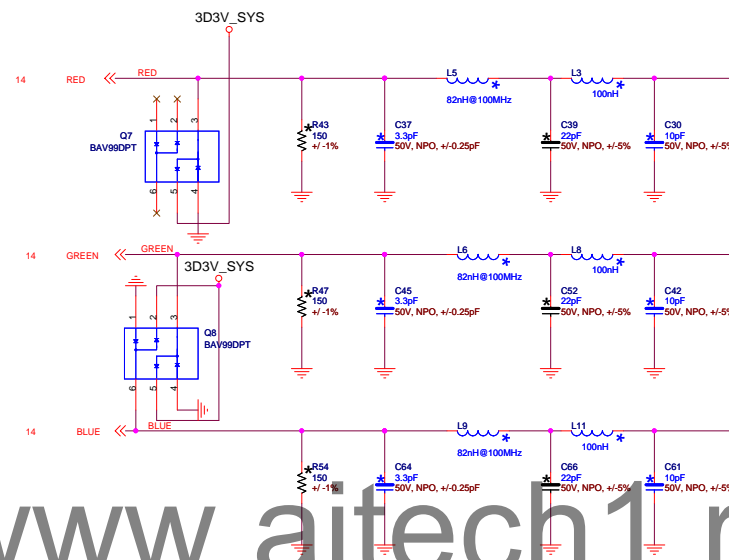
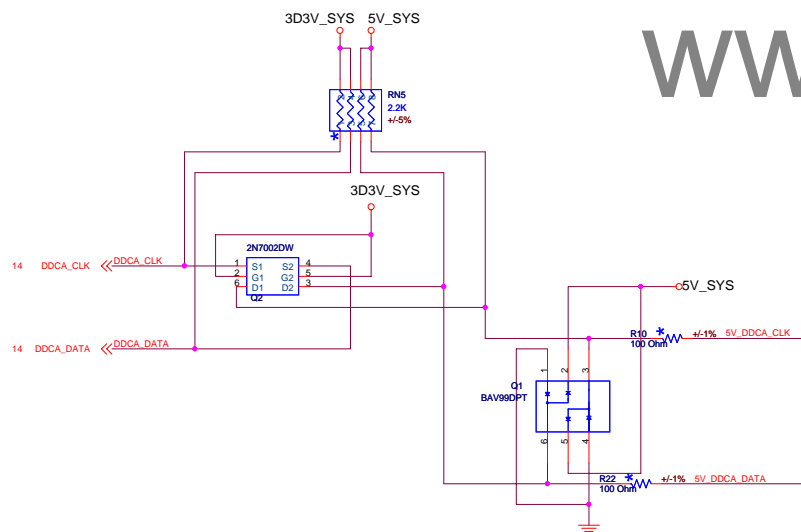
Change to another part.  
050608



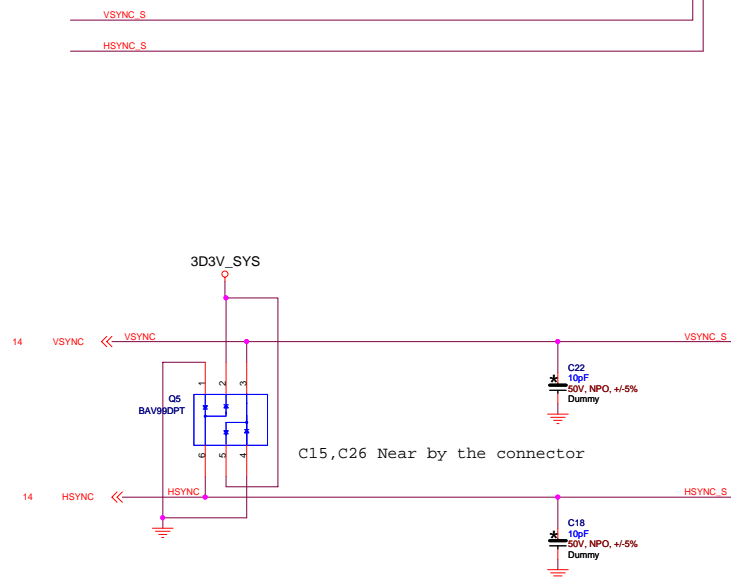


#### RGB routing

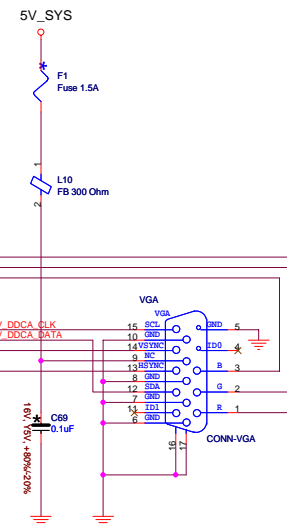
1. from GMCH to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced



The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.



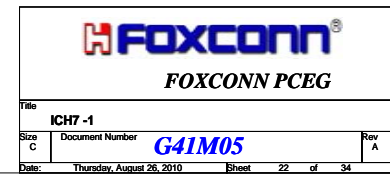
C15,C26 Near by the connector



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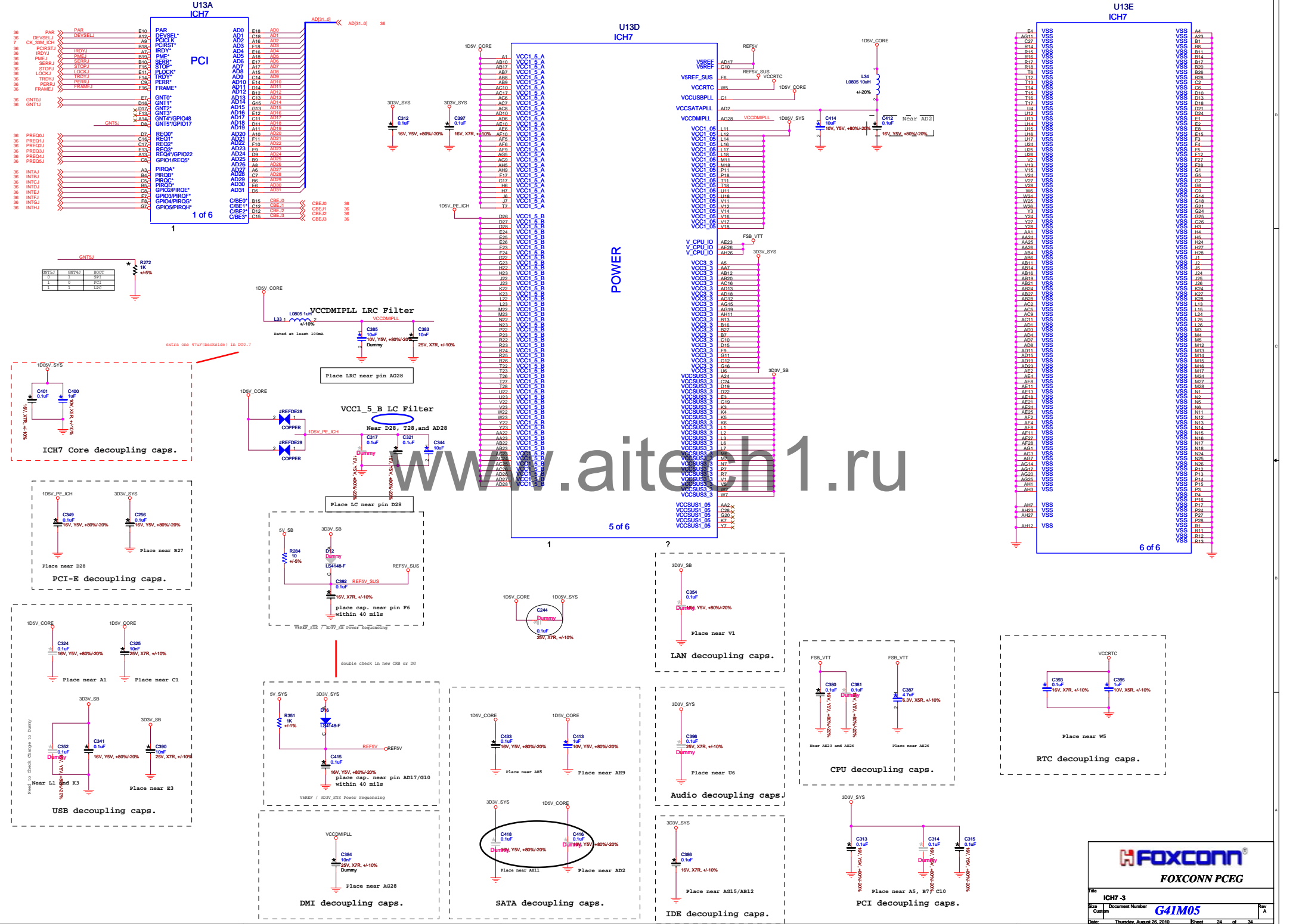
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double check unused GPIC  
pins



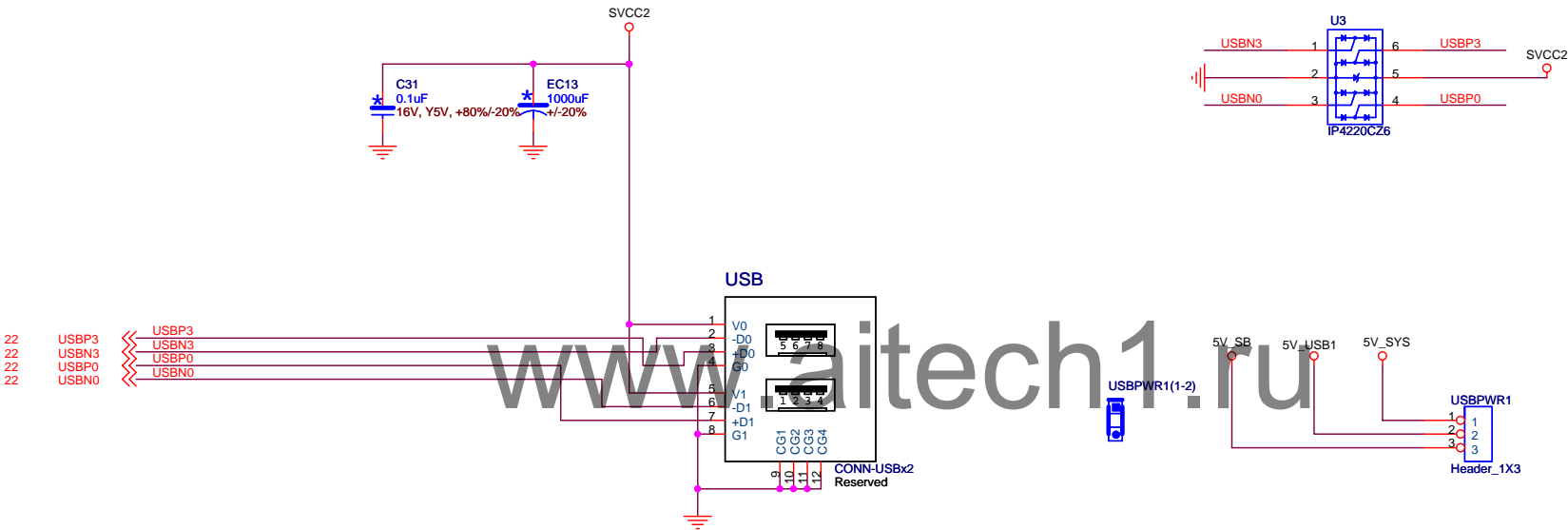




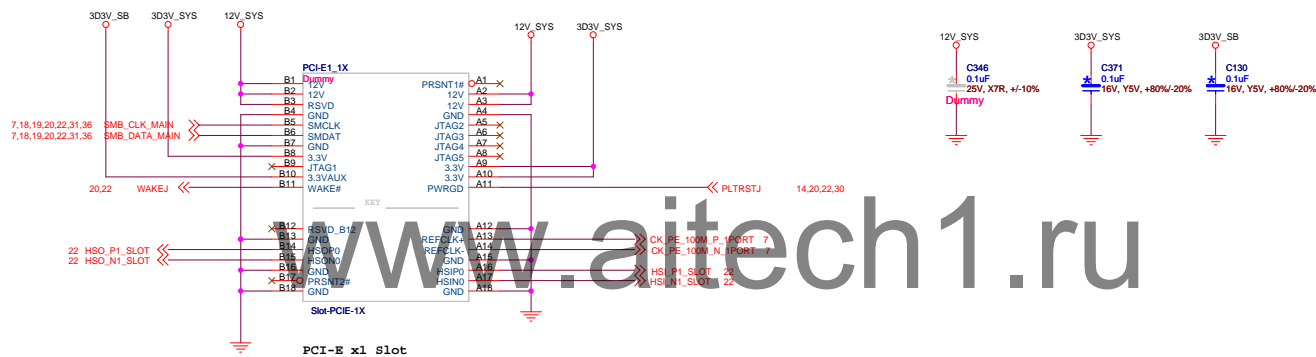


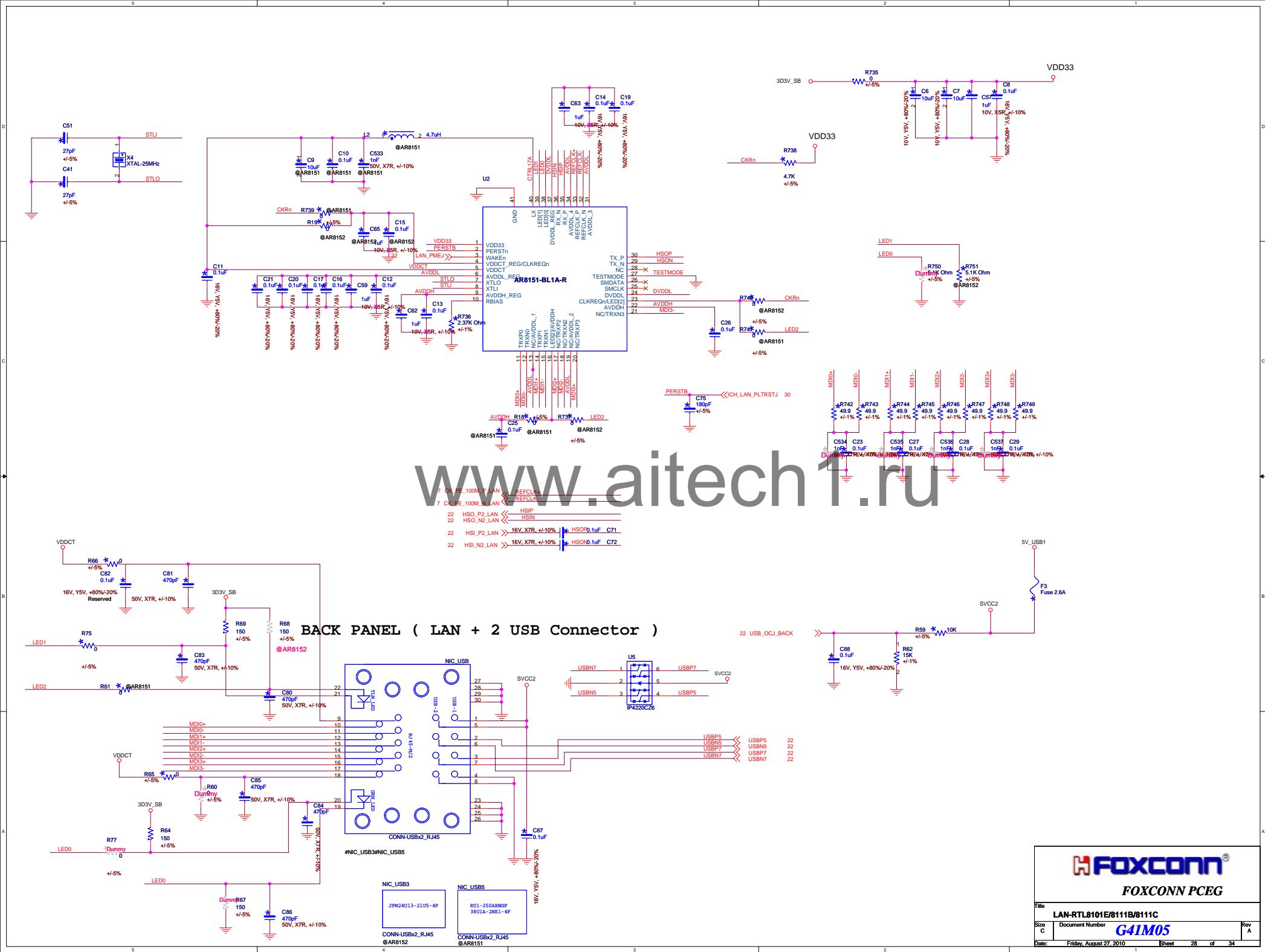


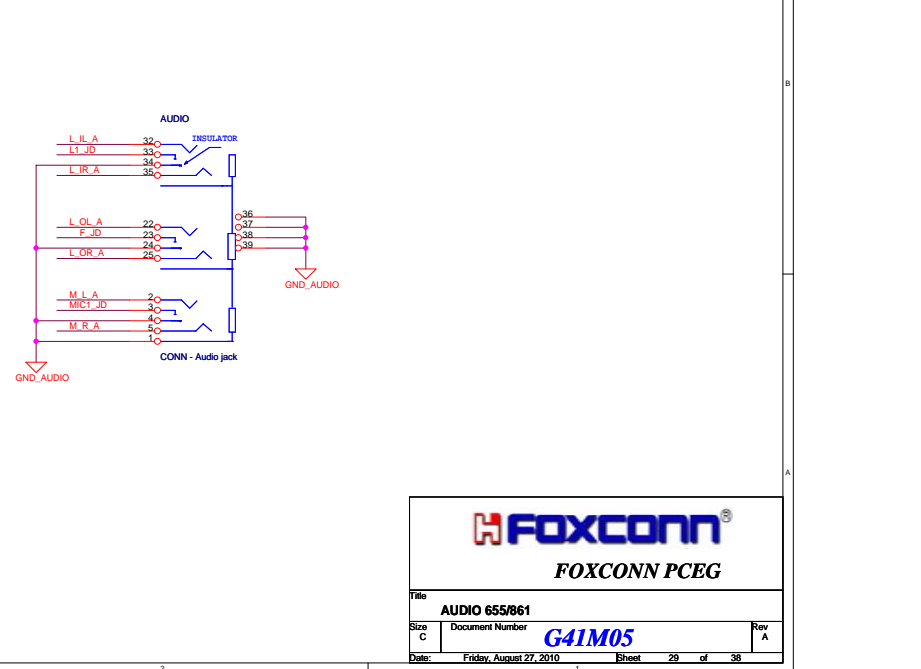
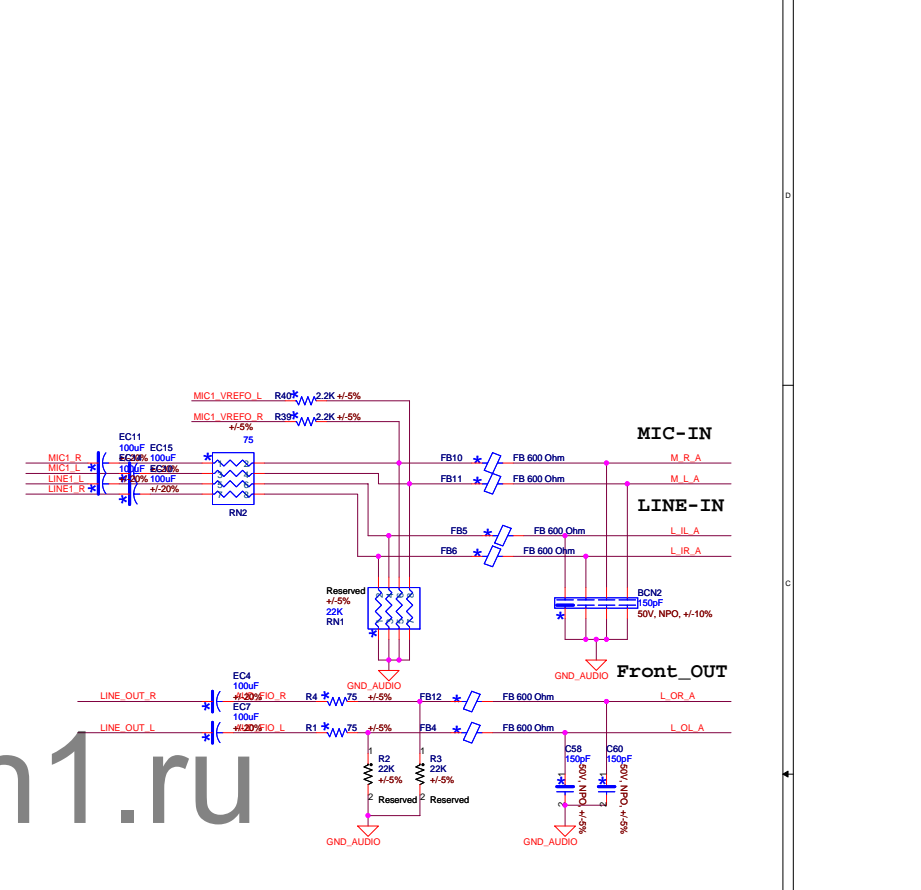
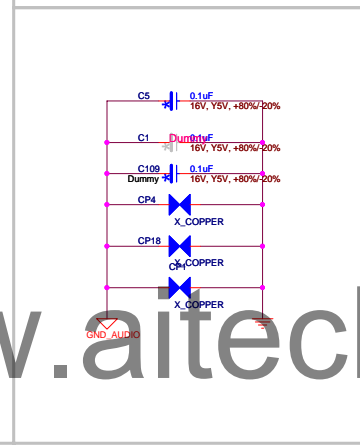
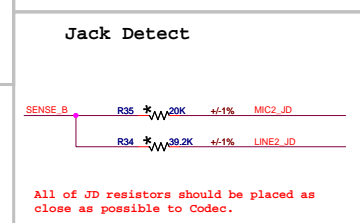
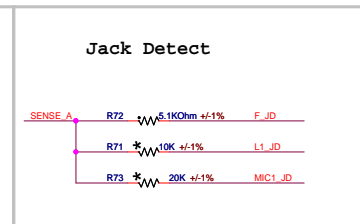
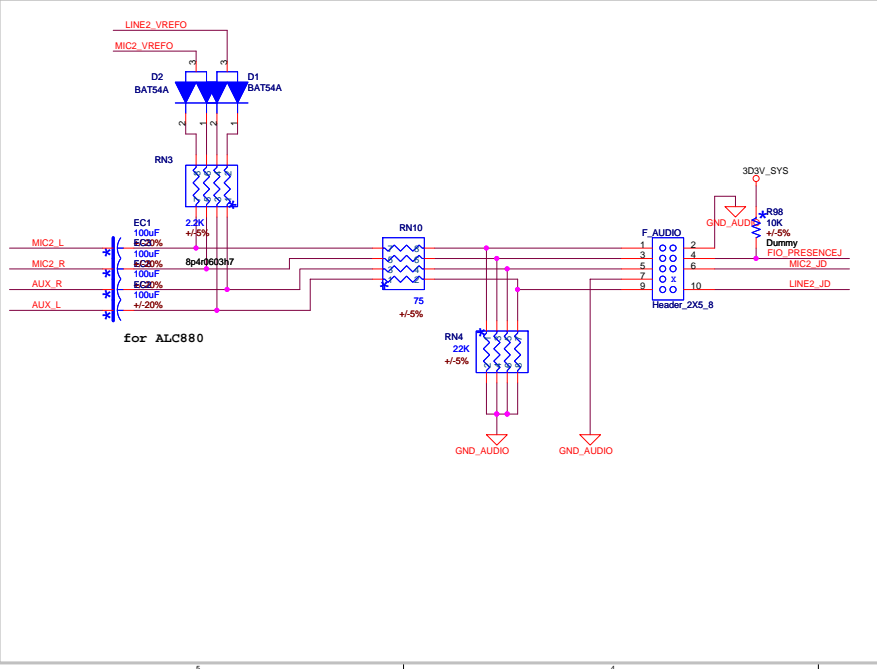
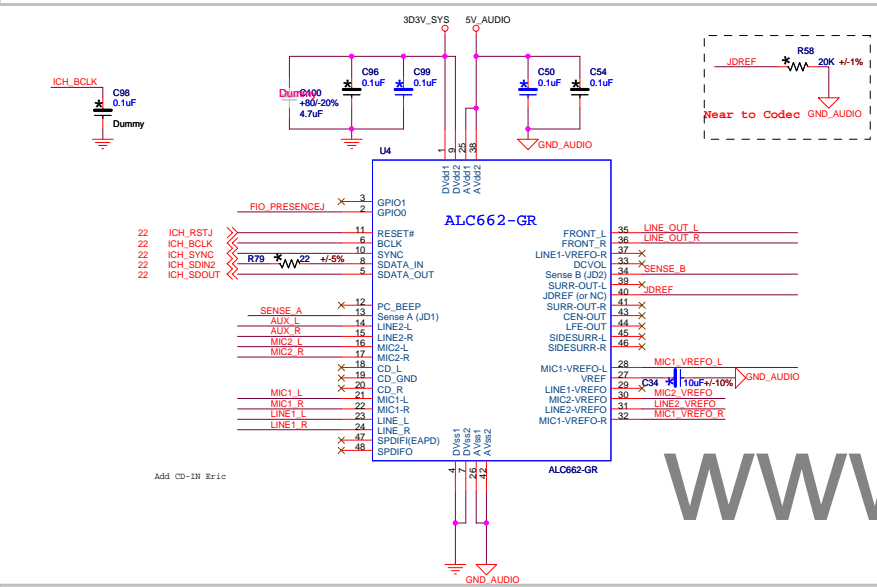
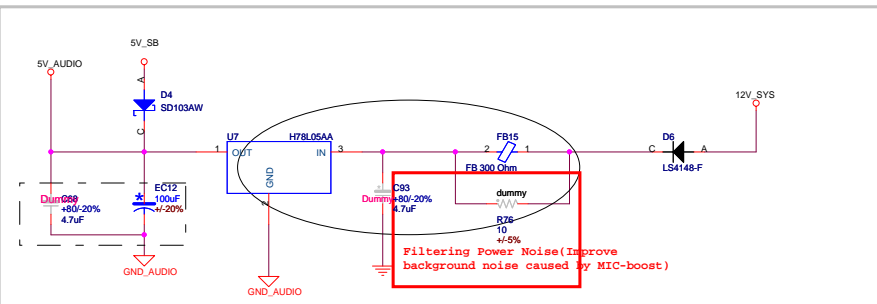
# Rear Dual USB Connector





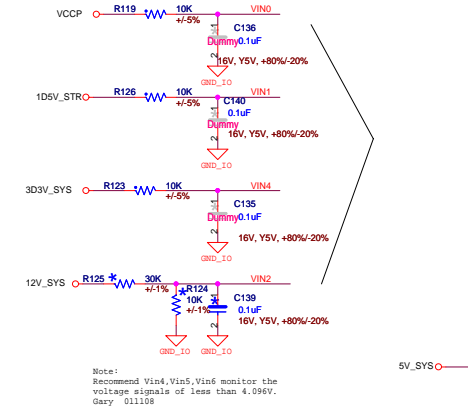






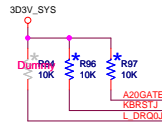
If without use these pins, Please pull-up to VCC.  
Don't let it floating

- 1.Pin 30:RESETCON#
- 2.Pin 95:VIN3/ATXPG
- 3.Pin 71:SUSB#
- 4..Power On Strapping Options pin
- 5.Please don't remove the pull-up resistor (R108) of pin38/LDRQ#.
- 6.Please don't remove any components in the VINx circuits and the FANx control circuits.
- 7.Please don't change the sequence of VIN0-VIN6.
- 8.If without use these pins,please pull-up to VCC, don't let it floating ,pin 3, pin 30, pin 38, pin 46, pin 95, pin 122, pin 124, pin 126.

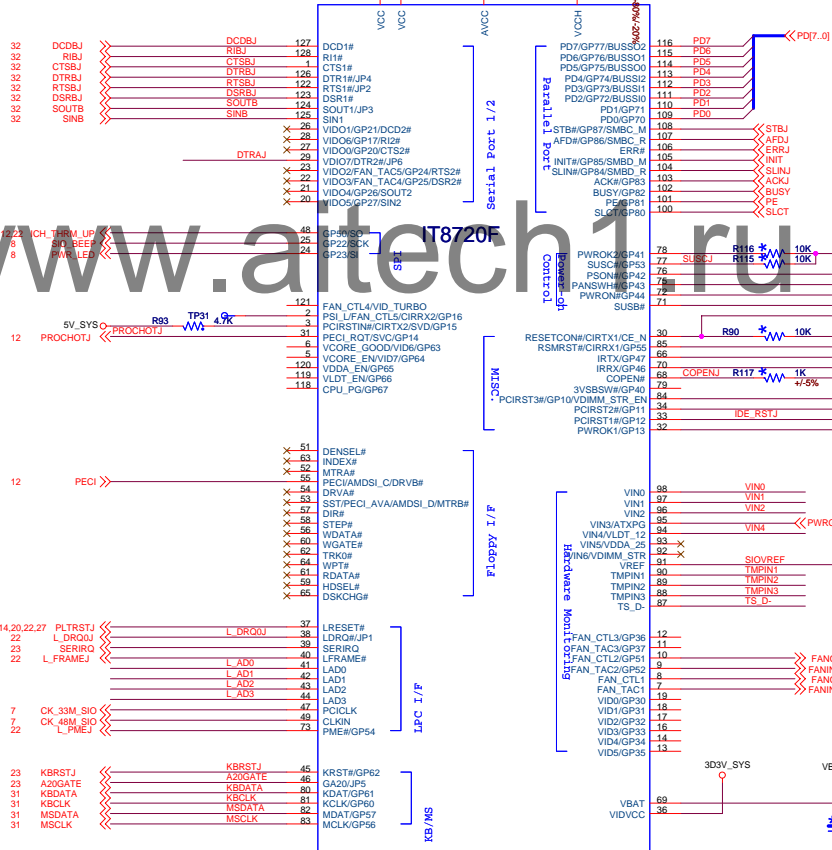
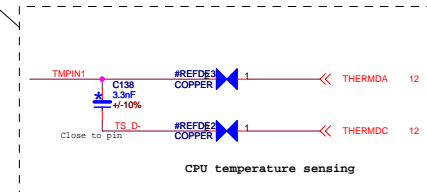
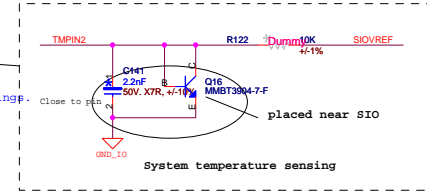


IT8720 Power On Strapping Options

JP1	Symbol	value	Description
Pin 38	Flashseg1_EN	1 Disabled.	
JP2	VIDO_EN	1 Disable VID output pins	
Pin 122		0 Enable VID output pins	
JP3	CHIP_SEL	Use for chip 1 when two I78718P exit in the same system, Chip is selected in conjunction with Global Configuration Register - Index 22, bit 7	
Pin 124			
JP4	K8PWR_EN	1 K8 power sequence function is disabled	
Pin 126		0 K8 power sequence function is enabled	
JP3 & JP5	FAN_CTL_SEL	11 The default value of EC Index 15h/16h/17h is 40h(Fan half speed)	
Pin 124 & 46		10 The default value of EC Index 15h/16h/17h is 7Fh(Fan off)	
		01 The default value of EC Index 15h/16h/17h is 00h(Fan full speed)	
		00 The default value of EC Index 15h/16h/17h is 20h	
JP5	WDT_EN	1 Disable WDT to rest PWROK	
Pin46		0 Enable WDT to rest PWROK	
JP6	SVID_EN	1 Disable SVID Function	
Pin29		0 Enable SVID Function	



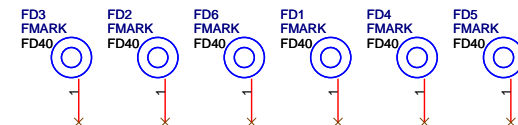
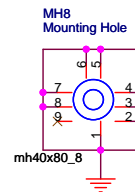
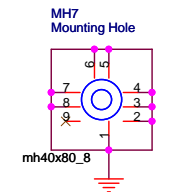
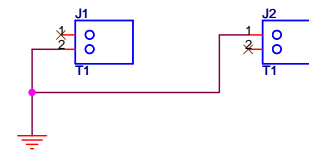
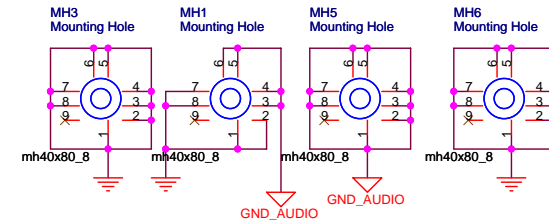
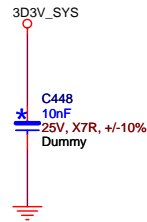
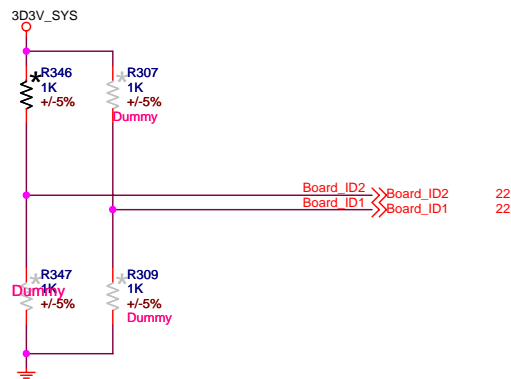
For the temperature sensor circuits,  
1)Please don't remove the 1uF capacitor(C620) between Vref and AGND.  
2)place R568 close to IT8720P.  
3)Keep the trace away from i2V, fast data bus, and CRTs.  
4)Recommended trace 10mils widths and 12 mils spacings.  
5)Isolate AGND and DGND.












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change C23 to 10uF follow Realtek advice. 11/28  
change EC5,EC12,EC14 to 6.3v/1000uF. 11/28


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CHANGE LIST		
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 <b>FOXCONN PCEG</b>		
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